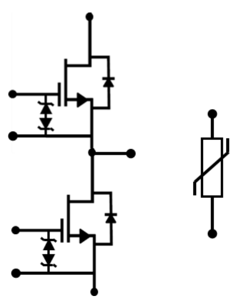
1200V-50A SiC Half-Bridge Module

Rev. B, February 2024

DATASHEET

UHB50SC12E1BC3N



Part Number	Package	Marking
UHB50SC12E1BC3N	E1B	UHB50SC12E1BC3N

Description

This SiC FET device is based on a unique ‘cascode’ circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device’s silicon-like gate-drive characteristics allows the use of unipolar gate drives, compatible with Si IGBTs, Si FETs, SiC MOSFETs or Si superjunction devices. Available in the E1B module package, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads, and any application requiring standard gate drive. Advanced Ag sintering die attach technology gives the module superior thermal performance.

Features

- On-resistance: $R_{DS(on)}$ = 19mΩ (typ)
- Operating temperature: 150°C (max)
- Excellent reverse recovery: Q_{rr} = 495nC
- Low body diode voltage: V_{FSD}= 1.2V
- Low gate charge: Q_G = 85nC
- Threshold voltage $V_{G(th)}$: 5V (typ) allowing 0 to 15V drive
- Low intrinsic capacitance
- ESD protected: HBM class 2 and CDM class C3

Typical applications

- EV charging
- PV inverters
- Switch mode power supplies
- Power factor correction modules
- Motor drives
- Induction heating

Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		1200	V
Gate-source voltage	V_{GS}	DC	-20 to +20	V
		AC (f > 1Hz)	-25 to +25	V
Continuous drain current [1]	I_D	T_C = 25°C	69	A
		T_C = 85°C	50	A
Pulsed drain current [2]	I_{DM}	T_C = 25°C	350	A
Power dissipation per switch	P_{tot}	T_C = 25°C	208	W
Maximum junction temperature	$T_{J,max}$		150	°C
Operating and storage temperature	T_J, T_{STG}		-55 to 150	°C

1. Limited by $T_{J,max}$
2. Pulse width t_p limited by $T_{J,max}$

Thermal Characteristics

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Thermal resistance, junction-to-case	$R_{\theta JC}$			0.46	0.6	°C/W

NTC Thermistor Characteristics

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Rated resistance	R_{25}	T_{NTC} = 25°C		5		kΩ
Resistance value tolerance	ΔR/R	T_{NTC} = 25°C	-5		5	%
Power dissipation	P_{25}	T_{NTC} = 25°C			20	mW
B constant	$B_{25/50}$	$R_2 = R_{25} \exp [B_{25/50} (1/T_2 - 1/(298.15\ K))]$		3375		K

Module

Parameter	Symbol	Test Conditions	Value	Units
Isolation voltage	V_{ISOL}	RMS, f = 50 Hz, t = 1 min	3	kV
Internal isolation			Al_2O_3	
Creepage distance		Terminal to heatsink	11.5	mm
		Terminal to terminal	6.3	mm
Clearance distance		Terminal to heatsink	10	mm
		Terminal to terminal	5	mm
Stray inductance module	L_{sCE}		11	nH

SiC FET Electrical Characteristics (T_J = +25°C unless otherwise specified)

Typical Performance - Static

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Drain-source breakdown voltage	BV_{DS}	V_{GS}=0V, I_D=4mA	1200			V
Total drain leakage current	I_{DSS}	V_{DS}=1200V, V_{GS}=0V, T_J=25°C		16	300	µA
		V_{DS}=1200V, V_{GS}=0V, T_J=150°C		50		
Total gate leakage current	I_{GSS}	V_{DS}=0V, T_J=25°C, V_{GS}=-20V / +20V		12	40	µA
Drain-source on-resistance	$R_{DS(on)}$	V_{GS}=12V, I_D=50A, T_J=25°C		19	24	mΩ
		V_{GS}=12V, I_D=50A, T_J=125°C		30		
		V_{GS}=12V, I_D=50A, T_J=150°C		35		
Gate threshold voltage	$V_{G(th)}$	V_{DS}=5V, I_D=20mA	4	5	6	V
Gate resistance	R_G	f=1MHz, open drain		2.2		Ω

Typical Performance - Reverse Diode

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Diode continuous forward current [1]	I_S	T_C = 25°C			69	A
Diode pulse current [2]	$I_{S,pulse}$	T_C = 25°C			350	A
Forward voltage	V_{FSD}	V_{GS}=0V, I_S=25A, T_J=25°C		1.2	1.4	V
		V_{GS}=0V, I_S=25A, T_J=150°C		1.4		
Reverse recovery charge	Q_{rr}	V_R=800V, I_S=50A, V_{GS}=-5V, R_{G_EXT}=20Ω, di/dt=4000A/µs, T_J=25°C		495		nC
Reverse recovery time	t_{rr}			21		ns
Reverse recovery charge	Q_{rr}	V_R=800V, I_S=50A, V_{GS}=0V, R_{G_EXT}=20Ω, di/dt=4000A/µs, T_J=150°C		465		nC
Reverse recovery time	t_{rr}			22		ns

Typical Performance - Dynamic

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Input capacitance	C_{iss}	V_{DS}=800V, V_{GS}=0V f=100kHz		2930		pF
Output capacitance	C_{oss}			187		
Reverse transfer capacitance	C_{rss}			3.3		
Effective output capacitance, energy related	$C_{oss(er)}$	V_{DS}=0V to 800V, V_{GS}=0V		240		pF
Effective output capacitance, time related	$C_{oss(tr)}$	V_{DS}=0V to 800V, V_{GS}=0V		533		pF
C_{OSS} stored energy	E_{oss}	V_{DS}=800V, V_{GS}=0V		77		μJ
Total gate charge	Q_G	V_{DS}=800V, I_D=50A, V_{GS} = -5V to 15V		85		nC
Gate-drain charge	Q_{GD}			19		
Gate-source charge	Q_{GS}			31		
Turn-on delay time	$t_{d(on)}$	Notes 3 and 4 V_{DS}=800V, I_D=50A, Gate Driver =-5V to +15V, R_{G_EXT}=10Ω, inductive Load, FWD: same device with V_{GS} = 0V and R_{G_EXT} =10Ω, T_J=25°C		22		ns
Rise time	t_r			18		
Turn-off delay time	$t_{d(off)}$			65		
Fall time	t_f			10		
Turn-on energy	E_{ON}			843		μJ
Turn-off energy	E_{OFF}			139		
Total switching energy	E_{TOTAL}			982		
Turn-on delay time	$t_{d(on)}$	Notes 3 and 4 V_{DS}=800V, I_D=50A, Gate Driver =-5V to +15V, R_{G_EXT}=10Ω, inductive Load, FWD: same device with V_{GS} = 0V and R_{G_EXT} =10Ω, T_J=150°C		22		ns
Rise time	t_r			16		
Turn-off delay time	$t_{d(off)}$			67		
Fall time	t_f			12		
Turn-on energy	E_{ON}			805		μJ
Turn-off energy	E_{OFF}			125		
Total switching energy	E_{TOTAL}			930		

3. Measured with the half-bridge mode switching test circuit in Figure 23.

4. A bus RC snubber (R_{BS} = 2.5Ω, C_{BS}=200nF) must be applied to reduce the power loop high frequency oscillations.

Typical Performance - Dynamic (continued)

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Turn-on delay time	$t_{d(on)}$	Notes 5 and 6, V_{DS}=800V, I_D=50A, Gate Driver =-5V to +15V, Turn-on $R_{G,EXT}$ = 2Ω, Turn-off $R_{G,EXT}$=2Ω, inductive Load, FWD: same device with V_{GS} = 0V and R_G = 2Ω, RC snubber: R_S=5Ω and C_S=150pF, T_J=25°C		32		ns
Rise time	t_r			24		
Turn-off delay time	$t_{d(off)}$			40		
Fall time	t_f			20		
Turn-on energy including R_S energy	E_{ON}			738		μJ
Turn-off energy including R_S energy	E_{OFF}			260		
Total switching energy	E_{TOTAL}			998		
Snubber R_S energy during turn-on	E_{RS_ON}			10		
Snubber R_S energy during turn-off	E_{RS_OFF}			5		
Turn-on delay time	$t_{d(on)}$	Notes 5 and 6, V_{DS}=800V, I_D=50A, Gate Driver =-5V to +15V, Turn-on $R_{G,EXT}$ = 2Ω, Turn-off $R_{G,EXT}$=2Ω, inductive Load, FWD: same device with V_{GS} = 0V and R_G = 2Ω, RC snubber: R_S=5Ω and C_S=150pF, T_J=150°C		30		ns
Rise time	t_r			21		
Turn-off delay time	$t_{d(off)}$			41		
Fall time	t_f			19		
Turn-on energy including R_S energy	E_{ON}			655		μJ
Turn-off energy including R_S energy	E_{OFF}			263		
Total switching energy	E_{TOTAL}			918		
Snubber R_S energy during turn-on	E_{RS_ON}			11		
Snubber R_S energy during turn-off	E_{RS_OFF}			5.5		

5. Measured with the chopper mode switching test circuit in Figure 24.

6. In this table, the switching energies (turn-on energy, turn-off energy and total energy) presented include the device RC snubber energy losses.

SiC FET Typical Performance Diagrams

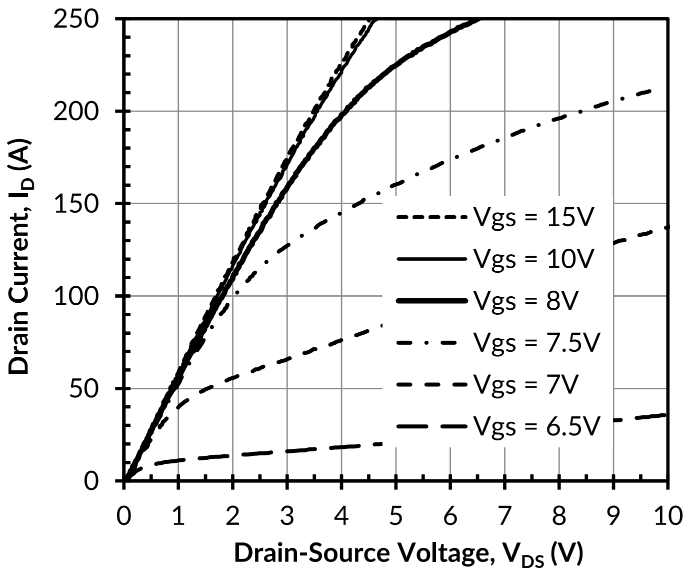


Figure 1. Typical output characteristics at T_J = - 55°C, tp < 250µs

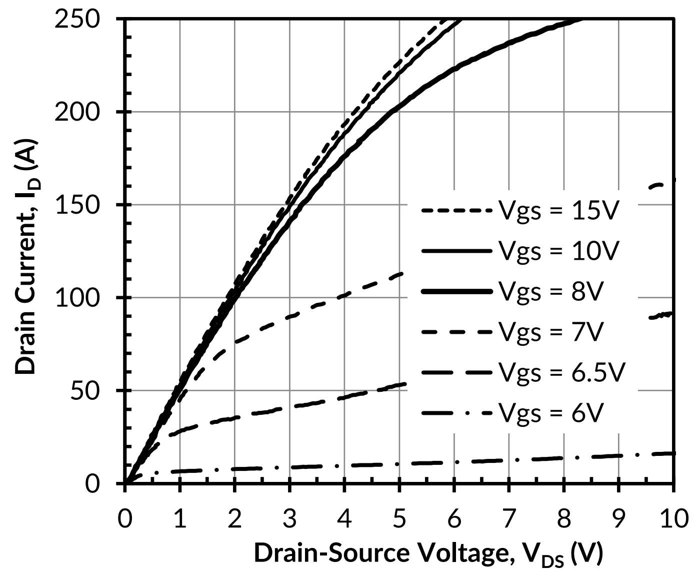


Figure 2. Typical output characteristics at T_J = 25°C, tp < 250µs

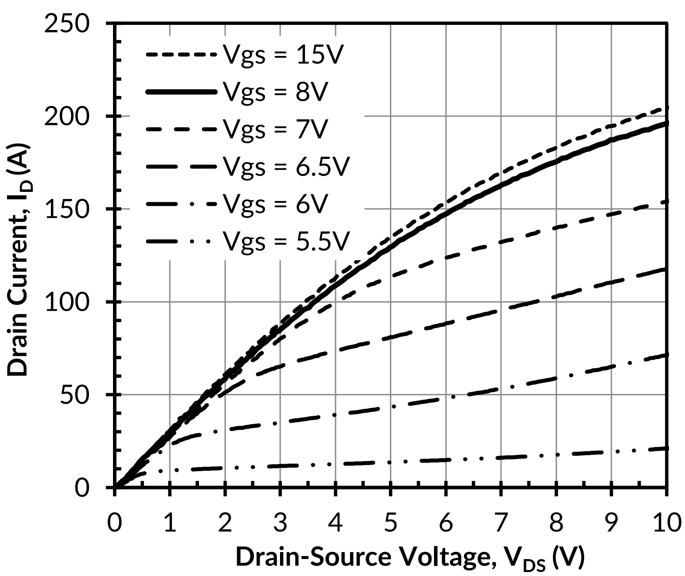


Figure 3. Typical output characteristics at T_J = 150°C, tp < 250µs

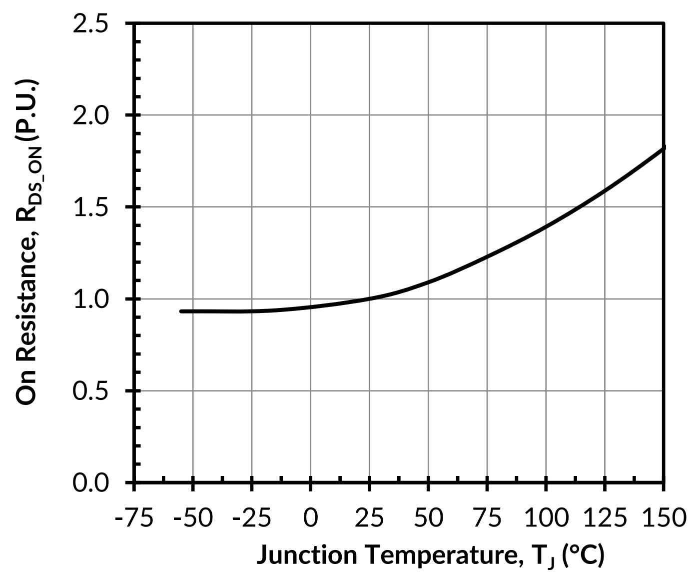


Figure 4. Normalized on-resistance vs. temperature at V_{GS} = 12V and I_D = 50A

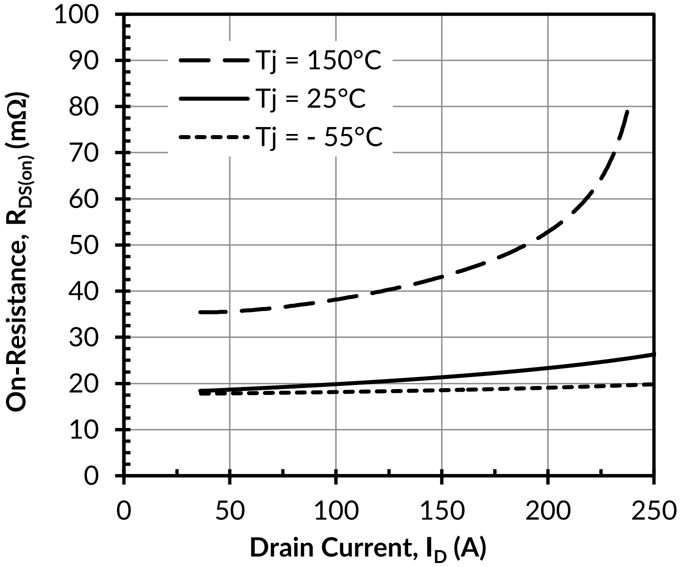


Figure 5. Typical drain-source on-resistances at V_{GS} = 12V

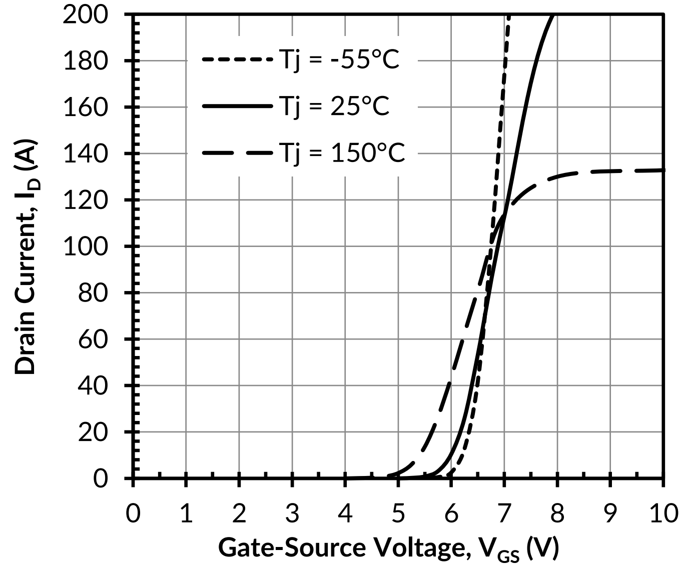


Figure 6. Typical transfer characteristics at V_{DS} = 5V

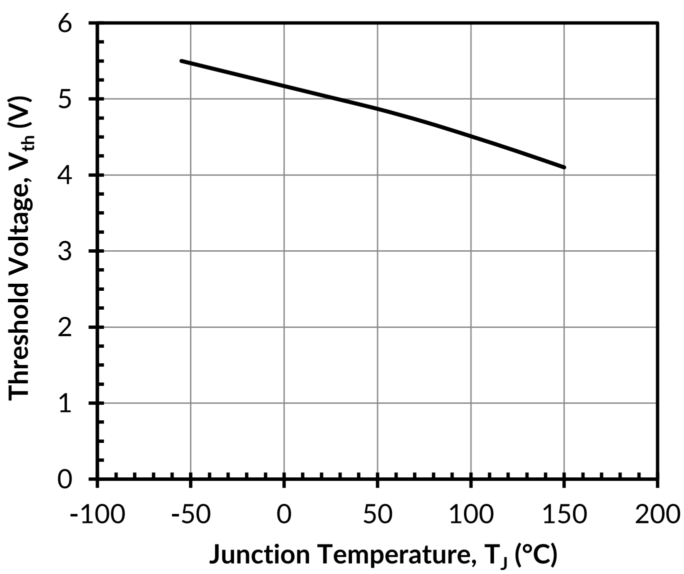


Figure 7. Threshold voltage vs. junction temperature at V_{DS} = 5V and I_D = 20mA

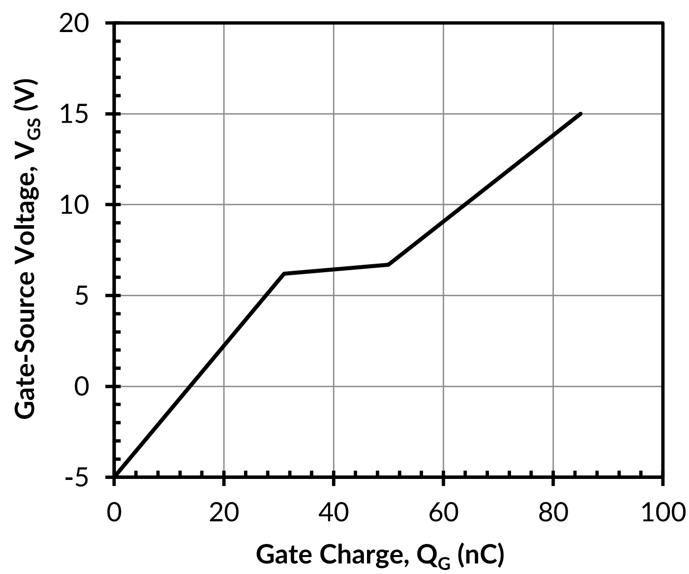


Figure 8. Typical gate charge at V_{DS} = 800V and I_D = 50A

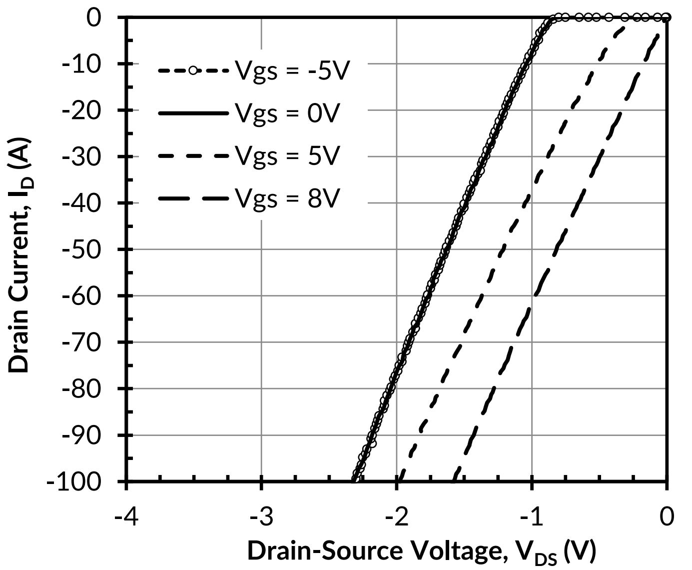


Figure 9. 3rd quadrant characteristics at T_J = -55°C

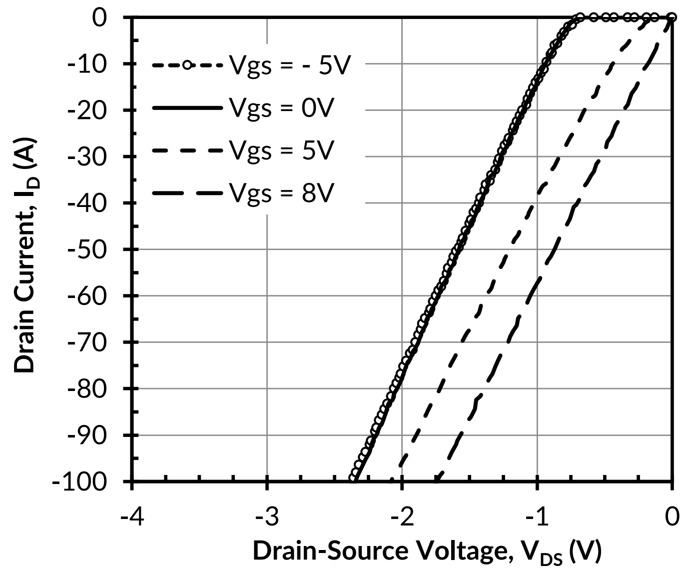


Figure 10. 3rd quadrant characteristics at T_J = 25°C

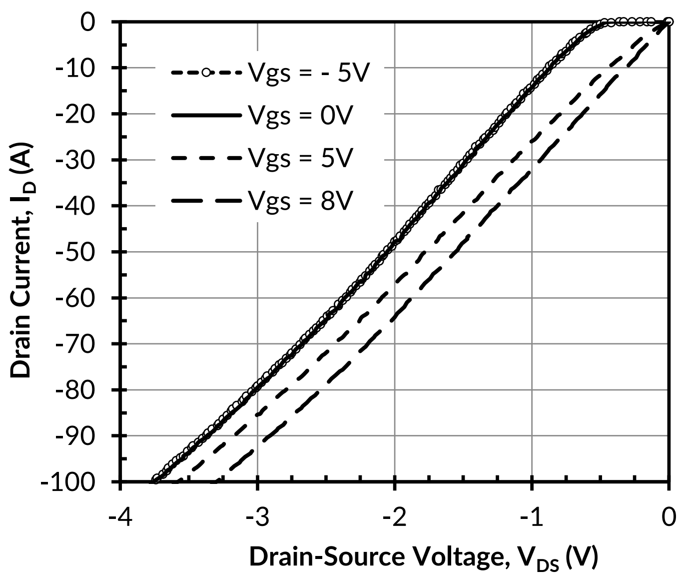


Figure 11. 3rd quadrant characteristics at T_J = 150°C

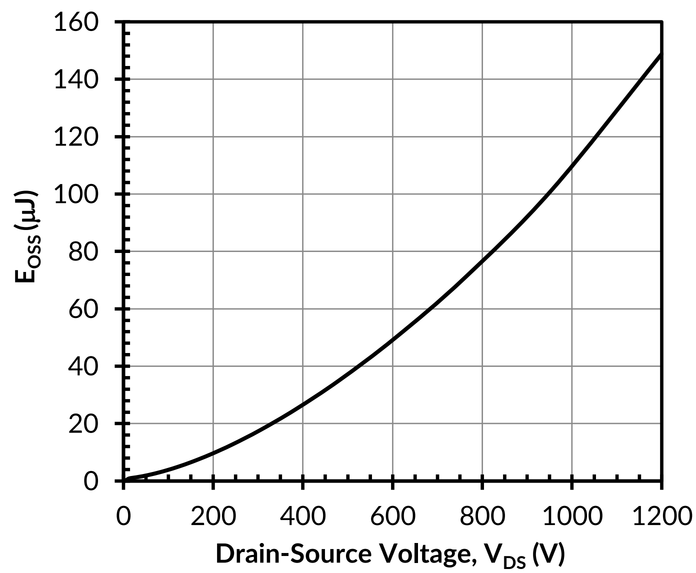


Figure 12. Typical stored energy in C_{OSS} at V_{GS} = 0V

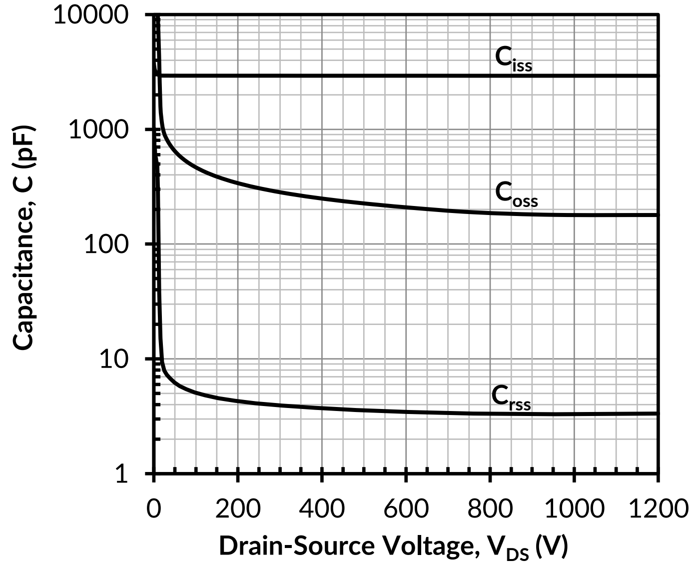


Figure 13. Typical capacitances at f = 100kHz and V_{GS} = 0V

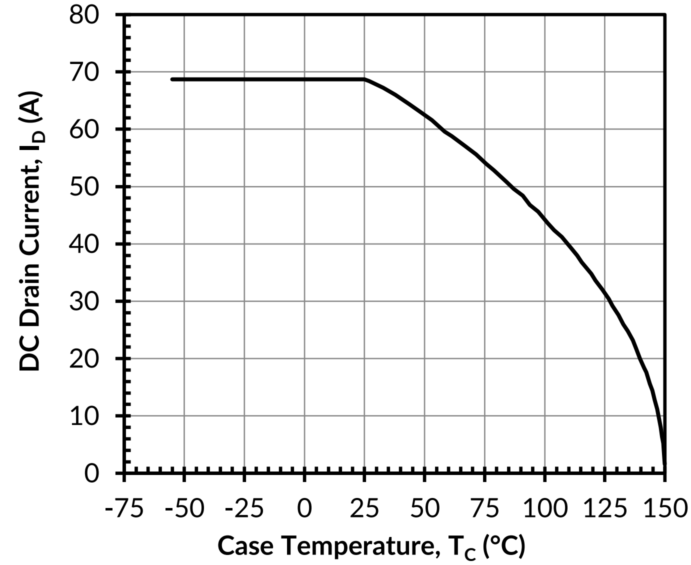


Figure 14. DC drain current derating

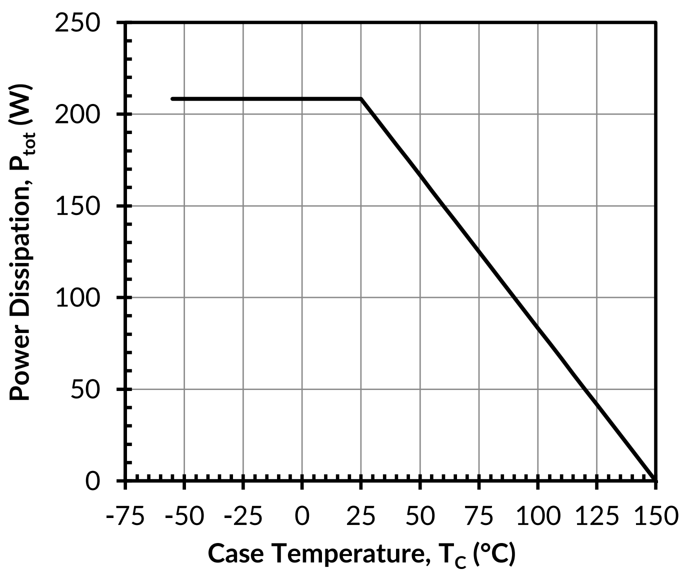
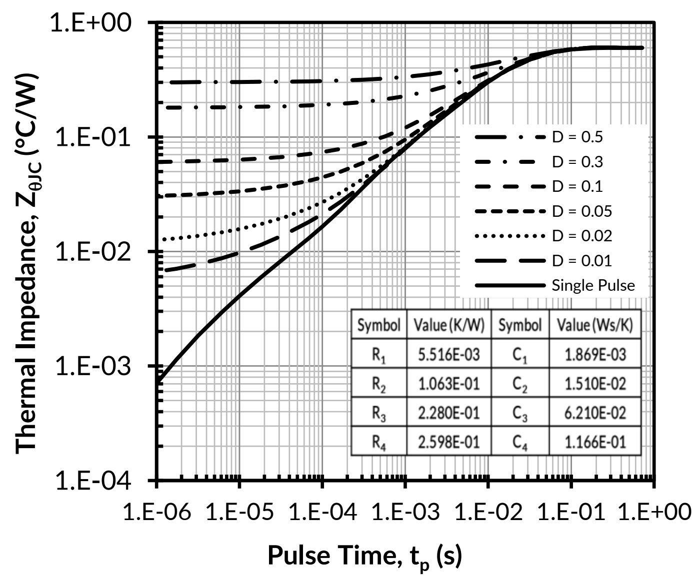


Figure 15. Total power dissipation



Symbol	Value (K/W)	Symbol	Value (Ws/K)
R_1	5.516E-03	C_1	1.869E-03
R_2	1.063E-01	C_2	1.510E-02
R_3	2.280E-01	C_3	6.210E-02
R_4	2.598E-01	C_4	1.166E-01

Figure 16. Maximum transient thermal impedance and parameters for thermal equivalent circuit (Foster) model

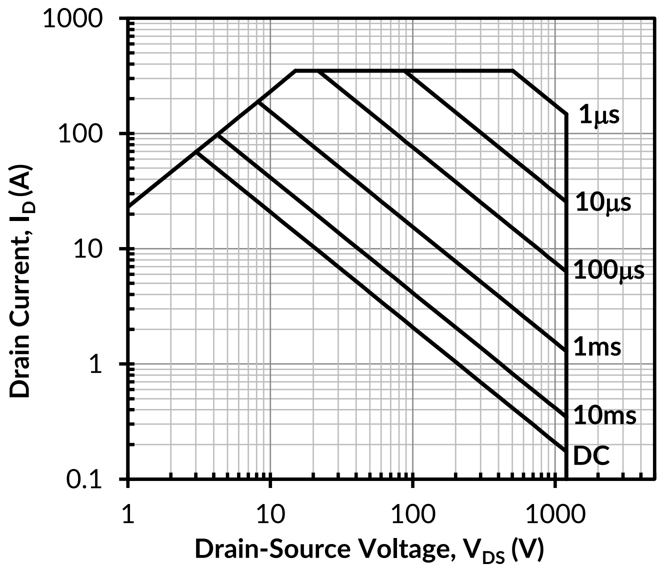


Figure 17. Safe operation area at T_C = 25°C, D = 0, Parameter t_p

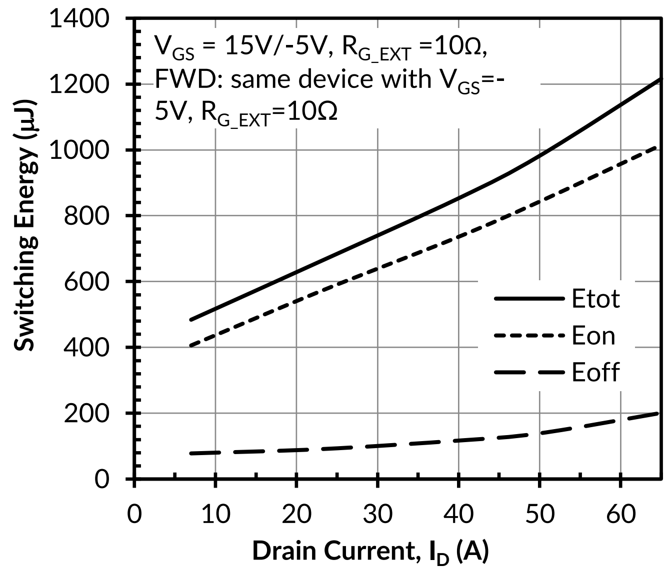


Figure 18. Clamped inductive switching energy vs. drain current at V_{DS} = 800V and T_J = 25°C

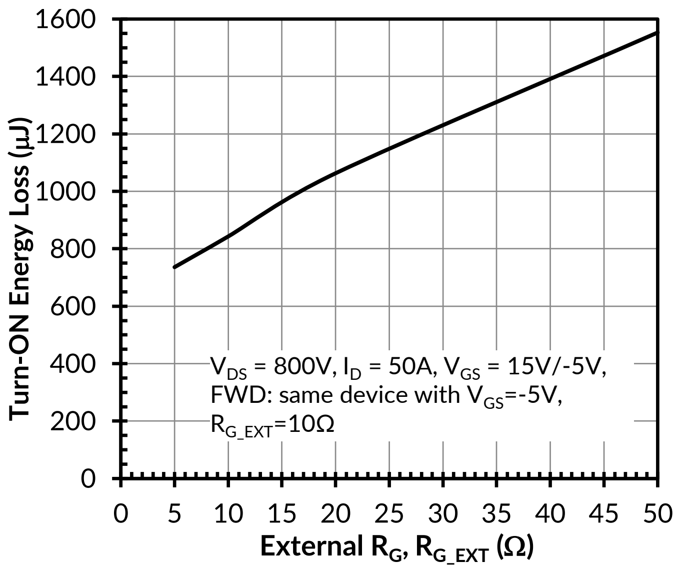


Figure 19. Clamped inductive switching turn-on energy vs. turn-on gate resistance R_G

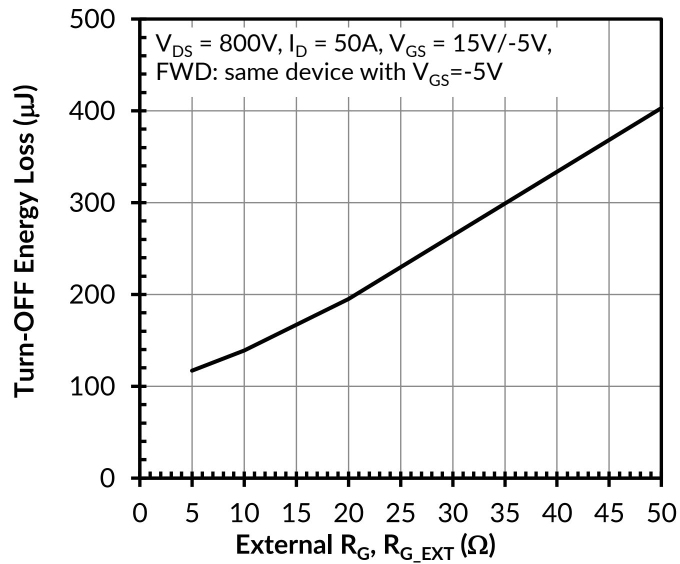


Figure 20. Clamped inductive switching turn-off energy vs. turn-off gate resitiance R_G

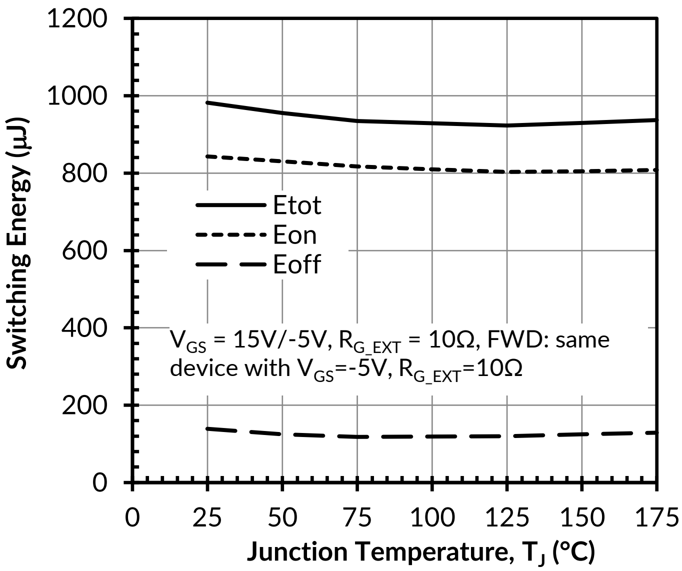


Figure 21. Clamped inductive switching energy vs. junction temperature at V_{DS} = 800V and I_D = 50A

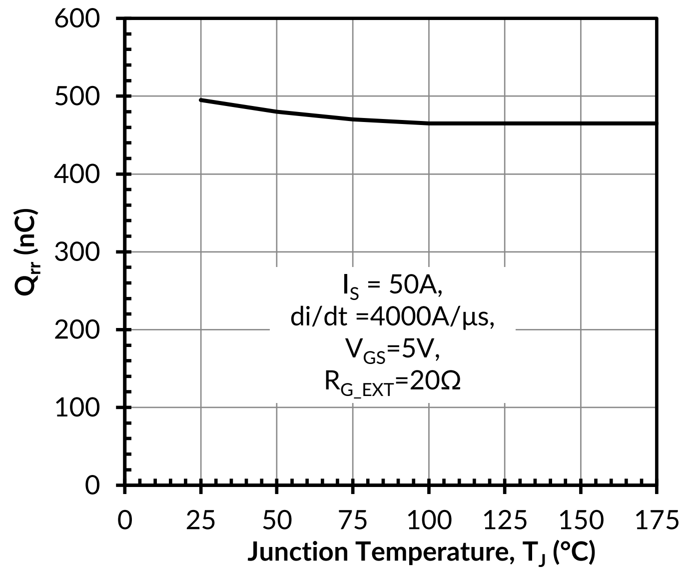


Figure 22. Reverse recovery charge Q_{rr} vs. junction temperature at V_{DS} = 800V

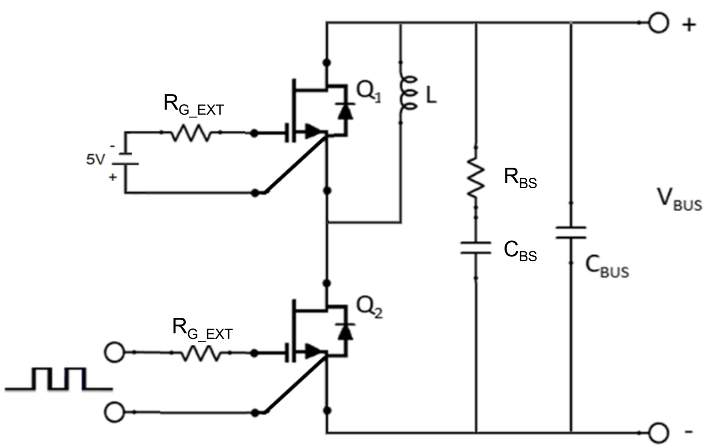


Figure 23. Schematic of the half-bridge mode switching test circuit. Note, a bus RC snubber (R_{BS} = 2.5Ω, C_{BS}=100nF) must be applied to reduce the power loop high frequency oscillations.

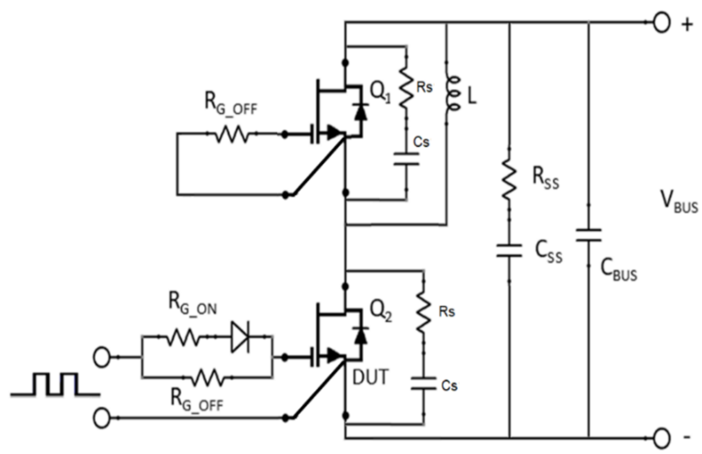
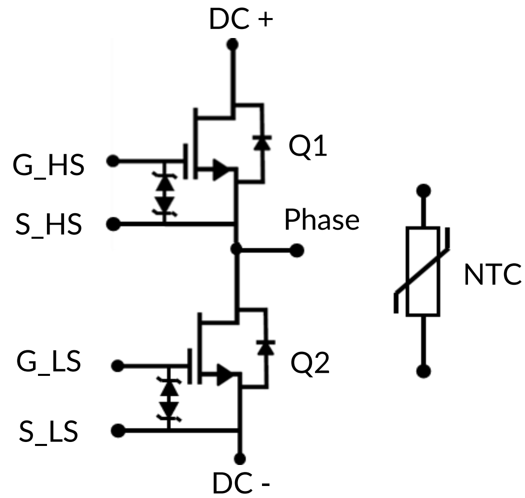
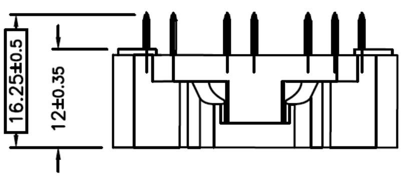
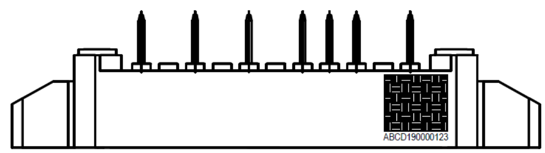


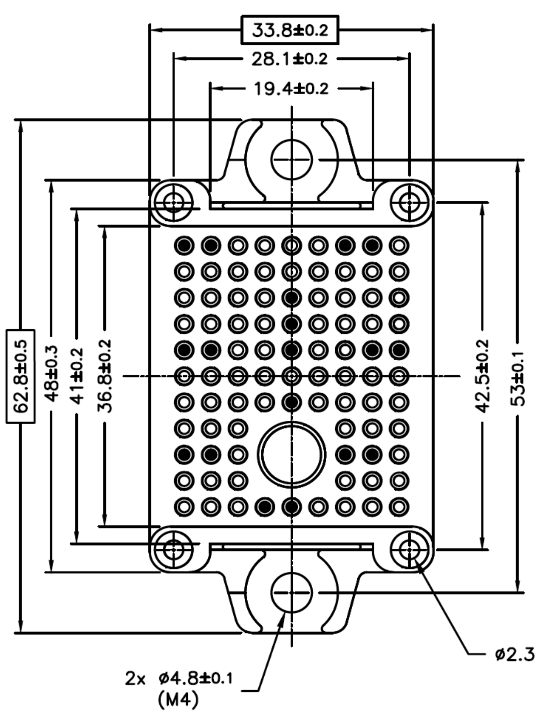
Figure 24. Schematic of the half-bridge mode switching test circuit with device RC snubbers (R_s =5Ω, C_s = 150pF) and a bus RC snubber (R_{SS} = 2.5Ω, C_{SS}=100nF).

Circuit Diagram and Pin Definitions

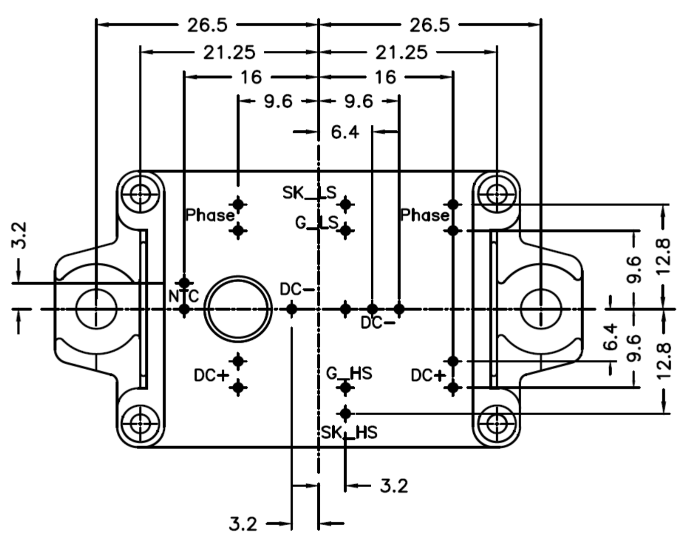








PCB HOLE PATTERN



NOTES:

1. All dimensions in millimeters (mm)
2. General tolerance: ± 0.1mm, unless otherwise specified

Important Mounting Information

This product is recommended for use with solder pin attach and phase change thermal interface materials, and not recommended for implementations using press fit and application of thermal grease. Please refer to mounting guidelines and user guide documents associated with this product for detailed information.

Applications Information

SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (C_{oss}), gate charge (Q_G), and reverse recovery charge (Qrr) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see https://www.qorvo.com/design-hub.

A snubber circuit with a small $R_{(G)}$, or gate resistor, provides better EMI suppression with higher efficiency compared to using a high $R_{(G)}$ value. There is no extra gate delay time when using the snubber circuitry, and a small $R_{(G)}$ will better control both the turn-off $V_{(DS)}$ peak spike and ringing duration, while a high $R_{(G)}$ will damp the peak spike but result in a longer delay time. In addition, the total switching loss when using a snubber circuit is less than using high $R_{(G)}$, while greatly reducing $E_{(OFF)}$ from mid-to-full load range with only a small increase in $E_{(ON)}$. Efficiency will therefore improve with higher load current. For more information on how a snubber circuit will improve overall system performance, visit the Qorvo website at https://www.qorvo.com/design-hub.

Important notice